## REMARKS

In the non-final Office Action, the Examiner rejected claims 21, 22, and 26 under 35 U.S.C. § 112, second paragraph, as indefinite; rejected claims 1, 3, 5-9, 11-18, and 26 under 35 U.S.C. § 102(b) as anticipated by Khosrowpour et al. (US Patent No. 5,734,329); rejected claims 10, 19, and 20 under 35 U.S.C. § 103(a) as unpatentable over Khosrowpour et al.; rejected claims 1, 2, 5-9, 11-18, 23, 24, and 26-29 under 35 U.S.C. § 102(b) as anticipated by Dickson et al. (U.S. Patent No. 5,644,700); and rejected claim 25 under 35 U.S.C. § 103(a) as unpatentable over Dickson et al. The Examiner objected to claim 4 as dependent upon a rejected base claim, but indicated that it would be allowable if rewritten in independent form to include all of the features of the base claim and any intervening claims. The Examiner indicated that claims 21 and 22 are allowable.

By this Amendment, Applicants amend claims 1, 20, and 26 to improve form. Applicants appreciate the Examiner's indication of allowable subject matter, but traverse the Examiner's rejections under 35 U.S.C. §§ 112, 102, and 103 with regard to the claims as now amended. Claims 1-29 remain pending.

At page 2 of the Office Action, the Examiner rejected claims 21, 22, and 26 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. The Examiner alleged that the claims are indefinite because the essential structural cooperative relationships between elements recited in the claim have been omitted (Office Action, page 2). Applicants respectfully traverse the rejection.

Applicants believe that the Examiner may have withdrawn this rejection with regard to claims 21 and 22 (which was also given in the last Office Action) because the Examiner

indicated that claims 21 and 22 are allowable (Office Action, page 12). If Applicants are incorrect in believing that the rejection of claims 21 and 22 under 35 U.S.C. § 112 is withdrawn, Applicants request clarification of the rejection of claims 21 and 22.

Claim 26 recites a control system that includes a bus. The system also includes several means-plus-function elements that perform an operation "on the bus." Applicants submit that the bus provides the necessary structural relationship between the means-plus-function elements.

In response to a similar argument presented by Applicants in the Amendment filed October 9, 2003, the Examiner reiterated that the essential structural cooperative relationships between the means of claim 26 have been omitted, resulting in a gap between the necessary structural connections (Office Action, page 8). Applicants continue to submit that the elements' relationship with the bus provides the structural relationships between the elements. Nevertheless, in order to expedite prosecution of this application, Applicants have amended claim 26 to recite that each of the recited means is connected to the bus. Accordingly, claim 26 is definite. Withdrawal of the rejection is, therefore, respectfully requested.

At pages 3-4 of the Office Action, the Examiner rejected claims 1, 3, 5-9, 11-18, and 26 as allegedly anticipated by Khosrowpour et al. Applicants traverse the rejection.

Amended claim 1, for example, recites a combination of features of a control system that includes a bus, a master device, and a plurality of slave devices. The master device connects to the bus and is configured to commence a bus cycle that includes an address interval and a data interval, provide a destination address on the bus during the address interval, and transmit or receive a command or data during the data interval. The slave devices connect to the bus and are configured to detect commencement of the bus cycle, begin to sample the destination address

from the bus a plurality of clock cycles after commencement of the address interval, and transmit or receive a command or data during the data interval.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either expressly or impliedly. Any feature not directly taught must be inherently present. See M.P.E.P. § 2131. Khosrowpour et al. does not disclose or suggest the features recited in claim 1. For example, Khosrowpour et al. does not disclose or suggest a plurality of slave devices that, among other things, begin to sample a destination address from the bus a plurality of clock cycles after commencement of an address interval, as recited in amended claim 1.

Instead, Khosrowpour et al. discloses that:

> the master sends a plurality of data bits forming a command, where each command includes at least one command bit and corresponding address bits. The slave device includes an output flip-flop for receiving and asserting the command bit. The memory of the slave device is preferably shift memory, which receives the data bits one at a time until filled with the address. Decode logic compares the address in the memory with a predetermined address or code, and enables the output flip-flop to receive the command bit if the address matches the predetermined code.

(col. 2, lines 31-41). Nowhere in this section, or elsewhere, does Khosrowpour et al. disclose or suggest a slave device that begins to sample a destination address from the bus a plurality of clock cycles after commencement of an address interval, as recited in amended claim 1.

The Examiner also appears to rely on the I2C bus specification for allegedly disclosing the features of claim 1 (Office Action, pages 3, 4, and 8-10). Applicants have reviewed the I2C bus specification and submit that the specification does not disclose or suggest a slave device that begins to sample a destination address from the bus a plurality of clock cycles after commencement of an address interval, as recited in amended claim 1.

If the Examiner persists with the rejection of claim 1 based on Khosrowpour et al. and/or the I2C bus specification, Applicants respectfully request that the Examiner particularly identify where Khosrowpour et al. and/or the I2C bus specification disclose a slave device that begins to sample a destination address from the bus a plurality of clock cycles after commencement of an address interval, as recited in amended claim 1. If the Examiner cannot identify where this feature is disclosed, the Examiner must withdraw the rejection.

For at least the foregoing reasons, Applicants submit that claim 1 is not anticipated by Khosrowpour et al. Claims 3, 5-9, and 11-16 depend from claim 1 and are, therefore, not anticipated by Khosrowpour et al. for at least the reasons given with regard to claim 1. Claims 3, 5-9, and 11-16 are also not believed to be anticipated by Khosrowpour et al. for reasons of their own.

For example, claim 3 recites that the bus includes multiplexed address and data signal lines configured to transport address, data, and commands, a cycle valid signal line configured to indicate a valid bus cycle, and a data/address interval signal line configured to differentiate the data interval from the address interval. Khosrowpour et al. does not disclose or suggest these features. For example, Khosrowpour et al. does not disclose or suggest a data/address interval signal line configured to differentiate the data interval from the address interval.

The Examiner alleged that Khosrowpour et al. discloses this feature and cited Figure 1A of Khosrowpour et al. for support (Office Action, page 4). Applicants disagree.

Khosrowpour et al. describes Figure 1A at column 4, lines 10-20, as:

> FIG. 1A illustrates some of the signals of the SMB 104. In particular, the SMB 104 includes data and clock signals according to the $I^2C$ bus standard by Phillips, and also includes a ground and M_PRESENT signal, along with a plurality of other signals as

> desired. The M_PRESENT signal is typically used both in systems according to prior art and according to the present invention for signaling to the slave devices 106a-d to indicate that the master 102 is present and powered on. The slave devices 106a-d correspondingly power up or down based on the status of the master device 102.

Nowhere in this section, or elsewhere, does Khosrowpour et al. disclose or suggest a data/address interval signal line, as recited in claim 3.

In response to a similar argument presented by Applicants in the Amendment filed October 9, 2003, the Examiner alleged that since the bus of Khosrowpour et al. is an I2C bus, it must strictly adhere to the I2C specification and the data line of the I2C bus is used to transmit several data bits implementing a command, where each bit is combined with clocking pulses and each command includes at least one command bit and a corresponding address bit (Office Action, pages 9-10). Regardless of the accuracy of the Examiner's allegation, the Examiner has not addressed the features of claim 3.

Claim 3 specifically recites, among other things, that the bus includes "a data/address interval signal line configured to differentiate the data interval from the address interval." In other words, claim 3 does not recite a data/address interval signal, but instead, a data/address interval signal line of the bus. The Examiner has provided no evidence that an I2C bus includes a data/address interval signal line. Instead, the Examiner has admitted something quite different:

> The I2C Bus physically consists of 2 active wires and a ground connection. . . . Only two lines (clock and data) are required for full duplexed communication between multiple devices

(emphasis added) (Office Action, page 3). Therefore, according to the Examiner the I2C bus does not include a data/address interval signal line.

In Fig. 1A, Khosrowpour et al. illustrates the lines of its server management bus (SMB) as including a data line, a clock line, a ground line, and an M_PRESENT line. Khosrowpour et

al. does not disclose that any of these lines is used to differentiate a data interval from an address interval.

For at least these additional reasons, Applicants submit that claim 3 is not anticipated by Khosrowpour et al.

Claim 13 recites that the master device is further configured to transmit a read-back signal to a destination device, receive a reply to the read-back signal, and determine the integrity of the destination device based on the received reply. Khosrowpour et al. does not disclose or suggest these features.

In response to similar arguments presented by Applicants in the Amendment filed October 9, 2003, the Examiner alleged that "it is clear from at least Fig. 1a that the M_PRESENT signal line (used for all communication purposes) performs the claimed function set forth in claim 13" (Office Action, page 10). Applicants disagree.

At column 4, lines 20-23, Khosrowpour et al. describes the M_PRESENT signal as:

> the M_PRESENT signal may be statically asserted high or low by the master device 102 for indicating to the slave devices 106a-d that the master device 102 is or is not present and powered on, respectively. The slave devices 106a-d correspondingly power up when the master device 102 is powered up. Alternatively, the M_PRESENT signal may be used to indicate to the slave devices 106a-d whether the master device 102 is present or not, indicating whether the slave devices should operate in slave mode or in stand-alone mode, respectively, based on the present status of the master device 102. Thus, the M_PRESENT signal is generally a static digital signal which is simply asserted low or high.
>
> In the communications system 100 according to the present invention, however, the master device 102 further includes means for sending commands to the slave devices 106a-d using the M_PRESENT signal line. In this manner, communication is established between the master device 102 and the slave devices 106a-d using the M_PRESENT signal line without otherwise affecting the static functionality. Furthermore, the communications are sent on an existing signal line, so that the cable incorporating the SMB 104 need not be modified.

Nowhere in this section, or elsewhere, does Khosrowpour et al. disclose or suggest that the M_PRESENT signal is used to transmit a read-back signal to a destination device, receive a reply to the read-back signal, and determine the integrity of the destination device based on the received reply, as recited in claim 13.

If the Examiner persists with this rejection based on Khosrowpour et al., Applicants respectfully request that the Examiner specifically identify where the features of claim 13 are disclosed by Khosrowpour et al. If the Examiner cannot identify where these features are disclosed, then the Examiner must withdraw the rejection.

For at least these additional reasons, Applicants submit that claim 13 is not anticipated by Khosrowpour et al.

Independent claim 17 recites features similar to features described above with regard to claim 1. Claim 17 is, therefore, not anticipated by Khosrowpour et al. for reasons similar to those given with regard to claim 1. Claim 18 depends from claim 17 and is, therefore, not anticipated by Khosrowpour et al. for at least the reasons given with regard to claim 17.

Amended independent claim 26 also recites features similar to features described above with regard to claim 1. Claim 26 is, therefore, not anticipated by Khosrowpour et al. for reasons similar to those given with regard to claim 1. Claim 26 is also not anticipated by Khosrowpour et al. for reasons of its own.

For example, claim 26 also recites means for sampling data on the bus a plurality of second clock signals after a start of the data interval. Khosrowpour et al. does not disclose or suggest this feature. For at least this additional reason, Applicants submit that claim 26 is not anticipated by Khosrowpour et al.

In view of the foregoing, Applicants respectfully request the reconsideration and withdrawal of the rejection of claims 1, 3, 5-9, 11-18, and 26 under 35 U.S.C. § 102 based on Khosrowpour et al.

At page 6 of the Office Action, the Examiner rejected claims 10, 19, and 20 under 35 U.S.C. § 103(a) as allegedly unpatentable over Khosrowpour et al. Applicants respectfully traverse the rejection.

Claims 10, 19, and 20 variously depend from claim 1 and 17. Claims 10, 19, and 20 are, therefore, patentable over Khosrowpour et al. for at least the reasons given with regard to claims 1 and 17. Claims 10, 19, and 20 are also believed to be patentable over Khosrowpour et al. for reasons of their own.

For example, claim 10 recites that a slave device is configured to sample a command or data on the bus 5 clock cycles after commencement of the data interval. Khosrowpour et al. does not disclose or suggest this feature.

The Examiner simply dismissed this feature, alleging that:

> using a particular number of cycles is an obvious design choice; and only involves routine skill in the art. In any event, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art

(Office Action, page 6). The Examiner's allegation lacks merit. The Examiner has provided absolutely no evidence that sampling a command or data on a bus 5 clock cycles after commencement of a data interval is obvious, let alone a design choice. Further, claim 10 does not relate to discovering an optimum value of a result effective variable. Therefore, the Examiner's "obvious design choice" argument lacks merit.

For at least these additional reasons, Applicants submit that claim 10 is patentable over Khosrowpour et al. Similar arguments can be made for claims 19 and 20 because the Examiner's allegation and the Khosrowpour et al. disclosure are similarly deficient.

In view of the foregoing, Applicants respectfully request the reconsideration and withdrawal of the rejection of claims 10, 19, and 20 under 35 U.S.C. § 103 based on Khosrowpour et al.

At pages 4-5 of the Office Action, the Examiner rejected claims 1, 2, 5-9, 11-18, 23, 24, and 26-29 under 35 U.S.C. § 102(b) as allegedly anticipated by Dickson et al. Applicants respectfully traverse the rejection.

Amended claim 1, for example, recites a combination of features of a control system that includes a bus, a master device, and a plurality of slave devices. The master device connects to the bus and is configured to commence a bus cycle that includes an address interval and a data interval, provide a destination address on the bus during the address interval, and transmit or receive a command or data during the data interval. The slave devices connect to the bus and are configured to detect commencement of the bus cycle, begin to sample the destination address from the bus a plurality of clock cycles after commencement of the address interval, and transmit or receive a command or data during the data interval.

Dickson et al. does not disclose or suggest the features recited in claim 1. For example, Dickson et al. does not disclose or suggest a plurality of slave devices that, among other things, begin to sample a destination address from the bus a plurality of clock cycles after commencement of an address interval.

At column 3, lines 7-26, Dickson et al. discloses the interaction of a master (SBMC) and a slave (SBS) as:

> The SBS 17, the SBMC's 18 and 19, and the SBS spectrum apparatus 21 comprise a maintenance subsystem which performs three major operations (i.e.,protocol). The beginning and ending "handshake", the slave signature packet and the information transfer data packet. With respect to the "handshake", the SBMC 18 or 19 initiates all links to the devices by asserting the INTERRUPT signal and sending a one byte "connect handshake" command. This command contains address data and a command code. The INTERRUPT signal is set until a response is received from the selected device or a connection timeout occurs. The communication link must be terminated with a "disconnect handshake". In order for the link to be successful, the SBS 17 must respond to the SBMC 18 with a "disconnect handshake" before releasing the bus 20 (i.e., disconnects).
>
> The "signature packet" comprises a unique address for each SBS connected to a single SBMC. When a matching address is found between an SBS and the "connect handshake" from the SBMC, the selected SBS responds with a message called the "signature packet".

(see also, col. 3, line 32 - col. 4, line 13). Dickson et al. does not disclose in these sections, or elsewhere, that a slave begins to sample a destination address from a bus a plurality of clock cycles after commencement of an address interval, as recited in amended claim 1.

In response to a similar argument by Applicants in the Amendment filed October 9, 2003, the Examiner alleged that:

> Contrary to Applicants' argument, it is inherent that the slave must "sample" the bus via SBS 17 in order to know whether its address is selected and begins to enable its transmit buffer and responds

(Office Action, page 11). Applicants submit that the Examiner is ignoring words in Applicants' claim 1. Claim 1 does not recite that the slave device simply samples a bus. Instead, claim 1 specifically recites that a slave device begins to sample the destination address from the bus a plurality of clock cycles after commencement of the address interval. Dickson et al. does not disclose or suggest this feature.

If the Examiner persists with the rejection of claim 1 based on Dickson et al., Applicants respectfully request that the Examiner particularly identify where Dickson et al. discloses a slave device that begins to sample a destination address from the bus a plurality of clock cycles after commencement of an address interval, as recited in amended claim 1. If the Examiner cannot identify where this feature is disclosed, the Examiner must withdraw the rejection.

For at least these reasons, Applicants submit that claim 1 is not anticipated by Dickson et al. Claims 2, 5-9, and 11-16 depend from claim 1 and are, therefore, not anticipated by Dickson et al. for at least the reasons given with regard to claim 1. Claims 2, 5-9, and 11-16 are also believed to be not anticipated by Dickson et al. for reasons of their own.

For example, claim 2 recites that the bus includes a plurality of redundant buses and the master device includes a plurality of redundant master devices, where each of the redundant master devices controls one of the redundant buses. Dickson et al. does not disclose or suggest these features. For example, Dickson et al. does not disclose or suggest redundant buses. Instead, Dickson et al. discloses only a single bus 20 (col. 2, lines 33-36).

The Examiner alleged that Dickson et al. discloses redundant buses and identified item 20 and the "bus shown in Fig. 1 for providing connection between 17 and 24 via 18, not labeled, perpendicular to bus 20" of Dickson et al. as corresponding to the redundant buses (Office Action, page 5). Applicants disagree. Item 20 of Dickson et al. appears to correspond to a bus (col. 2, lines 33-36). Applicants believe that the Examiner means the line shown connecting status bus slave apparatus 17 and primary status bus master controller 18 as the "bus shown in Fig. 1 for providing connection between 17 and 24 via 18, not labeled, perpendicular to bus 20." Dickson et al. does not disclose, suggest, or imply, however, that this line corresponds to a

redundant bus of bus 20. In fact, Dickson et al. does not disclose redundant buses at all and any allegation by the Examiner to the contrary finds no support in the Dickson et al. disclosure.

For at least these additional reasons, Applicants submit that claim 2 is not anticipated by Dickson et al.

Independent claims 17, 23, and 26 recite features similar to features described above with regard to claim 1. Claims 17, 23, and 26 are, therefore, not anticipated by Dickson et al. for reasons similar to those given with regard to claim 1. Claims 17, 23, and 26 are also believed to be not anticipated by Dickson et al. for reasons of their own.

For example, claim 23 recites, among other things, a plurality of redundant buses. As described above with regard to claim 2, Dickson et al. does not disclose or suggest this feature. For at least these additional reasons, Applicants submit that claim 23 is not anticipated by Dickson et al.

Claim 26 recites, among other things, means for sampling the data on the bus a plurality of second clock cycles after a start of the data interval. Dickson et al. does not disclose or suggest this feature. For at least these additional reasons, Applicants submit that claim 26 is not anticipated by Dickson et al.

Claims 18 and 24 depend from claims 17 and 23, respectively. Claims 18 and 24 are, therefore, not anticipated by Dickson et al. for at least the reasons given with regard to claims 17 and 23.

Independent claim 27 recites a combination of features of a multi-master system. The system includes a plurality of redundant buses, a plurality of slave devices connected to the buses, and at least first and second master devices connected to corresponding ones of the buses.

The first master device is configured to transmit a read-back signal to a destination device, receive a reply to the read-back signal, and determine the integrity of the destination device based on the received reply.

Dickson et al. does not disclose or suggest each of the features recited in claim 27. For example, Dickson et al. does not disclose or suggest a plurality of redundant buses for the reasons presented above with regard to claim 2.

For at least these reasons, Applicants submit that claim 27 is not anticipated by Dickson et al. Claims 28 and 29 depend from claim 27 and are, therefore, not anticipated by Dickson et al. for at least the reasons given with regard to claim 27. Claims 28 and 29 are also believed to not be anticipated by Dickson et al. for reasons of their own.

For example, claim 29 recites that the destination device includes the first master device. Dickson et al. does not disclose or suggest this feature. The Examiner did not address this feature and, therefore, did not establish a proper case of anticipation with regard to claim 29.

In view of the foregoing, Applicants respectfully request the reconsideration and withdrawal of the rejection of claims 1, 2, 5-9, 11-18, 23, 24, and 26-29 under 35 U.S.C. § 102 based on Dickson et al.

At pages 6-7 of the Office Action, the Examiner rejected claim 25 under 35 U.S.C. § 103(a) as allegedly unpatentable over Dickson et al. Applicants respectfully traverse the rejection.

Claim 25 depends from claim 23. Claim 25 is, therefore, patentable over Dickson et al. for at least the reasons given with regard to claim 23.

In view of the foregoing, Applicants respectfully request the reconsideration and withdrawal of the rejection of claim 25 under 35 U.S.C. § 103 based on Dickson et al.

In view of the foregoing amendments and remarks, Applicants respectfully request the Examiner's reconsideration of the application and the timely allowance of pending claims 1-29.

If the Examiner does not believe that all pending claims are now in condition for allowance, the Examiner is urged to contact the undersigned to expedite prosecution of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.

Paul A. Harrity
Reg. No. 39,574

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11240 Waples Mill Road
Suite 300
Fairfax, Virginia 22030
(571) 432-0800